SESSION 14 – TAPA I
Gate Dielectric Reliability

Wednesday, June 16, 3:25 p.m.
Chairpersons: R. Chau, Intel
H. Oyamatsu, Toshiba

14.1 — 3:25 p.m.

Impact of Boron Penetration from S/D-Extension on Gate-Oxide Reliability for 65-nm Node CMOS and Beyond, T. Yamashita, K. Ota, K. Shiga, T. Hayashi, H. Umeda, H. Oda, T. Eimori, M. Inuishi, Y. Ohji, K. Eriguchi*, K. Nakanishi*, H. Nakaoka*, T. Yamada*, M. Nakamura*, I. Miyanaga*, A. Kajiya*, M. Kubota*, and M. Ogura*, Renesas Technology Corp., Hyogo, Japan, *Matsushita Electric Industrial Co., Ltd., Kyoto, Japan

Performance of 65-nm node CMOSFETs is demonstrated. Plasma nitridation after gate etching is efficiently employed to suppress boron penetration from S/D-extension, which brings increase of gate leakage current and degradation of gate-oxide integrity for pMOSFET. Stress control from sidewall and interlayer insulator films is also found to be important to suppress the penetration. Transistors are optimized for LOP and LSTP device considering current drivability and gate-oxide integrity.

14.2 — 3:50 p.m.

Effects of Barrier Height (Φ_B) and the Nature of Bi-Layer Structure on the Reliability of High-k Dielectrics with Dual Metal Gate (Ru & Ru-Ta alloy) Technology, Y. H. Kim, R. Choi, R. Jha*, J.H. Lee*, V. Misra* and J. C. Lee, The University of Texas at Austin, Austin, TX, and *North Carolina State University, Raleigh, NC

We present the effects of barrier height on the reliability of HfO2 with dual metal gate technology in terms of Weibull slope, soft breakdown characteristics, defect generation rate, critical defect density and charge-to-breakdown. It was found that the lower Weibull slope of high-k dielectrics (compared to SiO2) is partially attributed to the lower barrier height of high-k dielectrics which in turn results in larger current increase. Thus, defect generation rate increases and charge-to-breakdown decreases, while critical defect density remains constant.

14.3 — 4:15 p.m.

On the Defect Generation and Low Voltage Extrapolation of Q_{BD} in SiO_2/HfO_2 Stacks, R. Degraeve, F. Crupi*, D.H. Kwak** and G. Groeseneken, IMEC, Leuven, Belgium, *University of Calabria, Italy **Samsung Electronics

Charge pumping on a SiO2/HfO2 stack is used to demonstrate that at least a part of the initially present traps is indistinguishable from the electrically generated traps. With this interpretation, we observe on our stack a trap generation threshold below which no degradation occurs, resulting in a virtually infinite QBD at low voltage.

14.4 — 4:40 p.m.

Significant Role of Cold Carriers for Dielectric Breakdown in HfSiON, I. Hirano, T. Yamaguchi, K. Sekine, M. Takayanagi, K. Eguchi, Y. Tsunashima, and H. Satake, Toshiba Corporation, Yokohama, Japan

Dielectric breakdown mechanisms in HfSiON were thoroughly investigated by utilizing the substrate hot carrier injection. It was found that the hole fluence dose not dominate the breakdown in HfSiON. Furthermore, it was experimentally clarified that the injected electrons into HfSiON have the significant role for the breakdown, irrespective of their potential energy. This result strongly suggest that the roles of injected cold electrons in HfSiON remarkably different from those inSiO2 and SiON.